IN THE SPECIFICATION

Please replace the paragraph at page 14, line 10, to page 15, line 17, with the following rewritten paragraph:

The adder circuit 13 includes logic circuits which are serially connected, for example. One input terminal of each logic circuit is supplied with the output Q of a corresponding one of the flip-flops 17. In this example, as the logic circuit, for example, a logic circuit capable of detecting coincidence/non-coincidence, for example, an exclusive logical OR (which is hereinafter referred to as Ex. OR) circuit 18 is used. One input terminal of the first-stage Ex. OR circuit 18 is supplied with the output Q of the first-stage flip-flop 17 and the other input terminal thereof is supplied with expected value correcting information "a". The expected value correcting information "a" is information output from an information output circuit and, for example, it is information programmed in the fuse 14 shown in the first embodiment. The expected value correcting information "a" is information which fixes the final output of the adder circuit 13 to expected value information having a preset value. Therefore, the final output becomes an error detection output j and when it is deviated from the preset value, occurrence of an error can be detected. In this example, a case wherein an odd number of flip-flops 17 are provided is shown as an example. In this cases, if transfer information i is "0", that is, if it is even ~~(if i = 2n)~~ (if i = a), the expected value correcting information "a" is set to "0". On the other hand, if transfer information i is "1", that is, if it is odd (Else), the expected value correcting information "a" is set to "1". As a result, the error detection output j is fixed at "0", that is, it is fixed at an even number ~~(j = 2k)~~ (j = 0). If the error detection output j is set at "1", that is, it is changed to an odd number, it is understood that information held in the transferring type register 11 is destroyed.